Georgia Tech College of Engineering
School of Electrical
and Computer Engineering

ECE 2020
Exam 1 Review

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September 17th, 2024

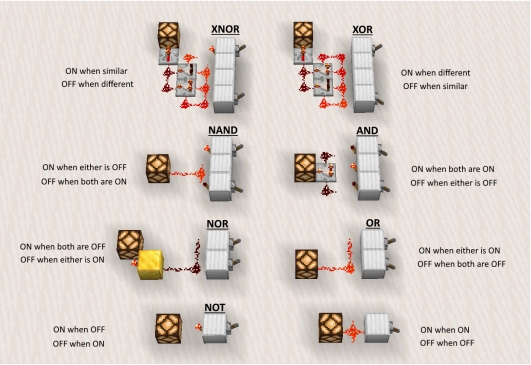
Logistics

- Now available:
  - HW 2—due September 17th **with optional 2 day extension** to Thursday, September 19th.
  - Lab report—due September 24th, 11:59pm
- Schedule for the next two weeks:
  - First exam, September 19th, in-class.

Agenda

Today's agenda

- HW1 review
- Puzzle review
- CMOS review
- Karnaugh maps
- SOP form



Source: r/minecraft

Agenda

- Today, September 10:
  - HW 1 review
  - Course schedule update
  - CMOS logic design review
  - Karnaugh maps and SoP forms
- Thursday, September 12: **Lab**—due Fri. Sep 20th, 11:59pm.
- Tuesday, September 17:
  - (Time permitting): Timing Diagrams (approx. half lecture)
  - Exam review (half lecture, and after class).

What to expect on the first exam

The exam will take 60 minutes and will be similar to homework assignments, but more brief and conceptual. There will be 3-4 problems

1. Boolean algebra and logic function simplification
2. Logic gates, operations, and circuits.
3. CMOS circuits

A single page of notes is permitted.

60%-70% HW1 material, 30%-40% HW2 material.

Lab 1 review

CMOS recap

PMOS/NMOS transistors

How to implement a logic function F in CMOS

Pull up network

- Implement the logic function F *as is*.
- Use PMOS transistors only.
- In practice: **complement all inputs**, i.e., design $F(\overline{A}, \overline{B}, \overline{C})$.

Pull down network

- Implement the complement of the logic function $\overline{F}$.
- Use NMOS transistors only.
- In practice: **keep inputs un-inverted**, i.e., design $\overline{F(A, B, C)}$.

Lab truth table

A	B	C	$B+C$	$\overline{B+C}$	Y
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	0	1

https://tinyurl.com/22jhm9on

CMOS Review

The systematic approach to CMOS design

Karnaugh Maps, Continued

Example from the ground up

Suppose you want to build a *digital system*. Suppose that you figure out how to express the thing that you want your system to **do in words** like this:

$$F = \begin{cases} 1 & \text{at least two inputs are false} \\ 0 & \text{otherwise} \end{cases}$$

You all now have the tools to design the entire system! Steps:

1. Find the simplest way to represent F using a K-map
2. Build a gate-level schematic for your design
3. Build a CMOS level schematic for your design

Big-picture example of Exam 1 material i

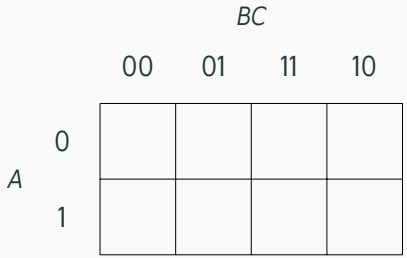
Truth table

$$F = \begin{cases} 1 & \text{at least two inputs are false} \\ 0 & \text{otherwise} \end{cases}$$

Step 1: construct truth table using word logic

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Big-picture example of Exam 1 material ii

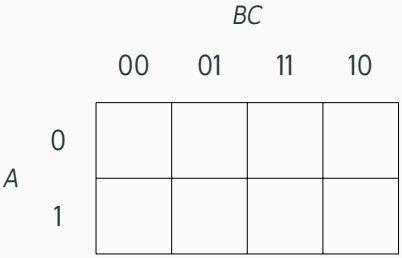


Step 2: Create an empty K-map to populate with your truth table.

K-maps

- It is up to your taste which variables to put on which side.
- Split your variables split to form a $2^{\#\text{inputs}}$ rectangle.
- The ordering of the binaries is called the "Gray code"

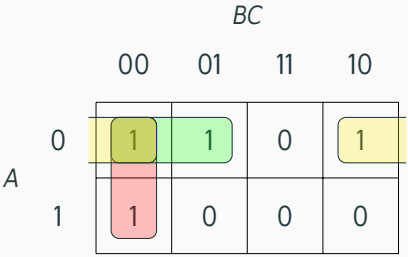
Big-picture example of Exam 1 material iii



Step 3: Populate your K-Map using Gray Coding.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Big-picture example of Exam 1 material iv



Step 4: Find the simplest form by grouping graphically:

$$F = \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{C} + \overline{B} \cdot \overline{C}.$$

K-maps

- It is up to your taste which variables to put on which side.
- Note the **"donut action"** creating the yellow group between m_0, m_2 squares across a 3rd dimension.
- **Warning:** You can only create 1s groups that sizes of powers of 2, e.g.: $1, 2, 4, \ldots$.

K-map example 2

Example 2

Using a K-map, simplify the following logic function:

$$F = \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C$$

Why? It's very difficult to do this with Boolean Algebra. Answer: $AB + BC + AC$

Note on “Don’t-Cares”

Gate level schematic

Gate-level schematic:

CMOS schematic

CMOS schematic:

HW1 review

HW1 Problem 1

Example: How to make HW1 Problem 1 in real life with CMOS

HW1 Problem 2

HW1 Problem 3