Digital System Design, Exam 3 (Fall 2024)

ECE 2020-IE
11/19/2024

Name: _____

I, _____, commit to uphold the ideals of honor and integrity by refusing to betray the trust bestowed upon me as a member of the Georgia Tech Community.

Please read this information:

- Please show all your work.
- Please box or circle your final answers.
- Please do not communicate with anyone or access the internet. Do your own work.
- You can use 1 standard sheet of letter-size paper as notes.
- This test has 2 problems that total up to 100 points.
- This test has 3 bonus questions that total up to 10 points.
- You have until the end of class to complete this exam.

Boolean Identities

- Identity:
  - $A + 0 = A$
  - $A \cdot 1 = A$
- Dominance:
  - $A + 1 = 1$
  - $A \cdot 0 = 0$
- Idempotence:
  - $A + A = A$
  - $A \cdot A = A$
- Inverse:
  - $A + \overline{A} = 1$
  - $A \cdot \overline{A} = 0$
- Commutative:
  - $A + B = B + A$
  - $A \cdot B = B \cdot A$
- Associative:
  - $A + (B + C) = (A + B) + C$
  - $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- Distributive:
  - $A \cdot (B + C) = A \cdot B + A \cdot C$
  - $A + B \cdot C = (A + B) \cdot (A + C)$
- Absorption:
  - $A \cdot (A + B) = A$
  - $A + A \cdot B = A$
- DeMorgan's:
  - $\overline{(A + B)} = \overline{A} \cdot \overline{B}$
  - $\overline{(A \cdot B)} = \overline{A} + \overline{B}$
- Double Complement:
  - $\overline{\overline{A}} = A$
- FOIL:
  - $(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$
- Disappearing Opposite:
  - $A + \overline{A} \cdot B = A + B$

Exam wrapper (2 bonus points)

Question I. (1 pts)

Reflect on your work in preparation for this course by answering the following questions:

1. Approximately how many hours did you spend studying for this exam? _____
2. Please indicate what percentage of your time was spent on the components of the course:
   (a) Prepared course notes: _____
   (b) Lecture slides and handwritten notes: _____
   (c) Solving and resolving homework: _____
   (d) Researching material on my own: _____

Question II. (1 pts)

Reflect on the topics you believed were your strengths and weaknesses going into this exam. You don't need to use every blank space.

1. Which topic(s) did you feel the most confident about?
   (a) _____
   (b) _____
   (c) _____
2. What topic(s) did you feel the least confident about?
   (a) _____
   (b) _____
   (c) _____

Problem 1: Sequential Logic Design (60pts)

Let $X(t) \in \{0, 1\}$ be a streaming binary input. The objective of this problem is to design a sequence detector that detects the string **101**. The binary output is $Z(t) \in \{0, 1\}$.
There are two possible ways to design this sequence detector:

1. **Overlapping case**: The last bit of a detected sequence becomes the first bit of the next sequence. ***Example***:

$$X(t) \to 0110101011001\ldots$$
$$Z(t) \to 0000101010000\ldots$$

2. **Non-overlapping case**: The last bit of a detected sequence does not become the first bit of the next sequence. ***Example***:

$$X(t) \to 0110101011001\ldots$$
$$Z(t) \to 0000100010000\ldots$$

Question 1a. (2 pts)

In both the overlapping and non-overlapping case, we need **three states** S_0, S_1, S_2. How many bits do we need to represent the three states with each type of encoding?

1. Number of bits required for **compact encoding**: _____
2. Number of bits required for **one-hot encoding**: _____

Question 1b. (3 pts)

Define the states as strings, and provide compact encoding and one-hot encoding representations of the states. You can use $\emptyset$ for the empty string. Multiple answers are possible for the encodings.

1. States as **strings**:

$$S_0 \to \_\_\_\_\_, \quad S_1 \to \_\_\_\_\_, \quad S_2 \to \_\_\_\_\_$$

2. States in **compact encoding**:

$$S_0 \to \_\_\_\_\_, \quad S_1 \to \_\_\_\_\_, \quad S_2 \to \_\_\_\_\_$$

3. States in **one-hot encoding**:

$$S_0 \to \_\_\_\_\_, \quad S_1 \to \_\_\_\_\_, \quad S_2 \to \_\_\_\_\_$$

Question 1c. (15 pts)

1. Draw **two Mealy state machines** using **compact encoding**—one for the **overlapping case** of the sequence detector, and one for the **non-overlapping case** of the sequence detector. (12pts)
2. Label your drawings to indicate which is the overlapping case and which is the non-overlapping case, and write 1 sentence to explain the difference. (3pts)

Recall: In a Mealy Machine, the output depends on the present state and the present input.

Question 1d. (20 pts)

1. Fill in the state transition table below for the **non-overlapping case** of the 101 sequence detector with **compact encoding**. (10pts)
2. Derive simplified Boolean expressions for the future state bits Q_1^+ and Q_0^+, and the output signal Z. (You don't necessarily have to use the K-maps). (10pts)

Q_1	Q_0	X	Q_1^+	Q_0^+	Z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Q_1Q_0

X \	00	01	11	10
0				
1				

Q_1Q_0

X \	00	01	11	10
0				
1				

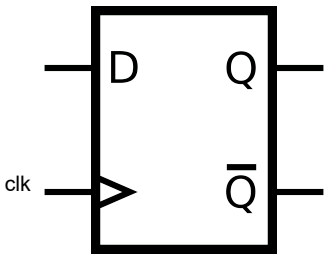
Q_1Q_0

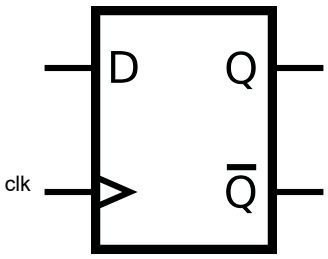
X \	00	01	11	10
0				
1				

Question 1e. (20 pts)

1. Using your results from Question 1d, draw a sequential logic circuit that implements the non-overlapping case of the 101 sequence detector with compact encoding using the two D flip-flops shown below. (15pts)

2. Label where the **present state bits**, the **future state bits**, and the **output** is located in your drawing. (5pts)





Problem 2: Flip-Flops (40pts)

The symbol for a *D flip-flop* is shown below in Figure 1.

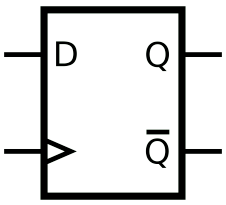


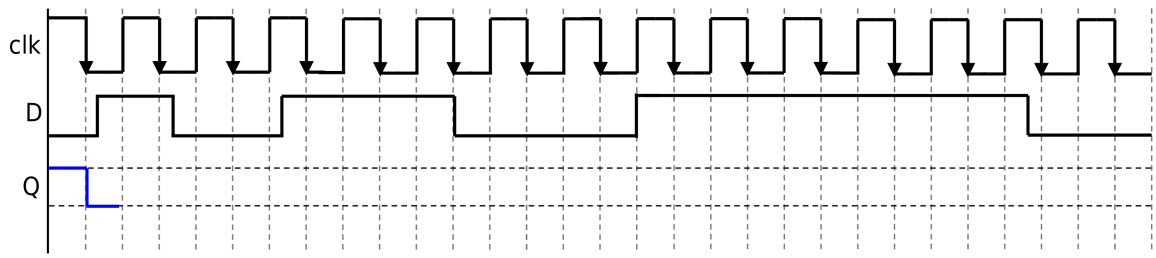
Figure 1: The symbol for a Data flip-flop, or "D" flip-flop

Question 2a. (5 pts)

In two sentences or less, explain what functions a *D* flip-flop has (there are 2):

Question 2b. (15 pts)

Complete the timing diagram below for a **falling-edge triggered** *D* flip-flop.



The symbol for a *JK flip-flop* is shown below in Figure 2.

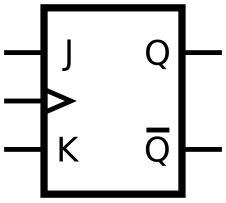


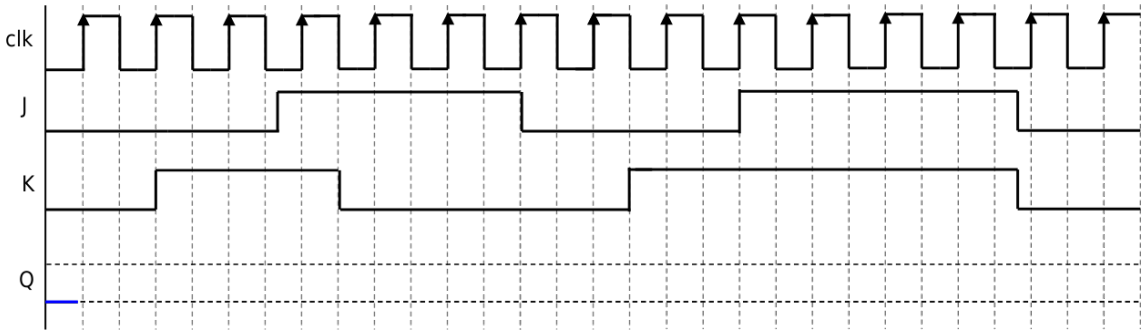
Figure 2: A JK flip-flop

Question 2c. (5 pts)

In 2 sentences or less, explain what functions a JK flip-flop has (there are 4).

Question 2d. (15 pts)

Complete the timing diagram below for a **rising-edge triggered** JK flip-flop.



Bonus: All New™ Flip-Flop (8pts)

You want to design a new flip-flop with two inputs X and Y, and a clock input clk.

1. If $XY = 00$, Q toggles with each clock pulse
2. If $XY = 01$, Q becomes 1 at the next pulse
3. If $XY = 10$, Q becomes 0 at the next pulse
4. If $XY = 11$, Q toggles with each clock pulse

Question III. (8 pts)

Draw a state diagram for the new flip-flop described above. You may use either a Moore or Mealy model for the state diagram. You can treat the state Q as the output.

Scratch paper; if used, please clearly indicate which question you are working on