Digital System Design, Exam 2 (Fall 2024)

ECE 2020-IE
10/17/2024-10/19/2024

Name: ________________________________

I, ________________________________, have neither given nor received unauthorized help on this exam, and I have conducted myself within the guidelines of the honor code of the Georgia Institute of Technology.

Please read this information:

- This is a 48-hour take home exam.
- Do not collaborate or communicate with anyone during the time period of this exam. You are on your honor.
- You are responsible for the content of all your answers.
- Please show all your work.
- Please box or circle your final answers.

Boolean Identities

- Identity:
  - $A + 0 = A$
  - $A \cdot 1 = A$
- Dominance:
  - $A + 1 = 1$
  - $A \cdot 0 = 0$
- Idempotence:
  - $A + A = A$
  - $A \cdot A = A$
- Inverse:
  - $A + \overline{A} = 1$
  - $A \cdot \overline{A} = 0$
- Commutative:
  - $A + B = B + A$
  - $A \cdot B = B \cdot A$
- Associative:
  - $A + (B + C) = (A + B) + C$
  - $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- Distributive:
  - $A \cdot (B + C) = A \cdot B + A \cdot C$
  - $A + B \cdot C = (A + B) \cdot (A + C)$
- Absorption:
  - $A \cdot (A + B) = A$
  - $A + A \cdot B = A$
- DeMorgan's:
  - $\overline{(A + B)} = \overline{A} \cdot \overline{B}$
  - $\overline{(A \cdot B)} = \overline{A} + \overline{B}$
- Double Complement:
  - $\overline{\overline{A}} = A$
- FOIL:
  - $(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$
- Disappearing Opposite:
  - $A + \overline{A} \cdot B = A + B$

Exam wrapper (1 bonus point)

Question I. (1 pts)

Reflect on your work in preparation for this course by answering the following questions:

1. Approximately how many hours did you spend studying for this exam?
2. Please indicate what percentage of your time was spent on the components of the course:
   (a) Prepared course notes: _______
   (b) Lecture slides and handwritten notes: _______
   (c) Solving and resolving homework: _______
   (d) Researching material on my own: _______

Problem 1: Building blocks and trading with advice (30pts)

Suppose that you are electronically monitoring the price of a stock, and you have access to predictions from *multiple algorithms* $P_0, P_1, P_2 \dots$ where

$$P_k = \begin{cases} 1 & \text{if algorithm } k \text{ predicts the price will increase} \\ 0 & \text{otherwise,} \end{cases} \tag{1}$$

for each algorithm $k = 0, 1, 2, \dots$. In this problem we will design an enhanced trading device that leverages these *multiple predictors*. To achieve this, we define a logic function

$$M = \begin{cases} 1 & \text{if the majority predict the price is increasing} \\ 0 & \text{otherwse.} \end{cases} \tag{2}$$

Question 1a. (5 pts)

Suppose that there are three prediction signals P_0, P_1, and P_2. Fill in the below truth table for M.

P_2	P_1	P_0	M
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Question 1b. (5 pts)

Write M in sum-of-products (SOP) form, indicating the minterms, and draw a circuit that implements M using a decoder and a single logic gate.

Question 1c. (5 pts)

Now, suppose there are 4 price predictors P_0, P_1, P_2, and P_3. Notice that there is now a possibility that a *tie can occur*. Let B be the logic of a *tie-breaker*, where

$$B = \begin{cases} 1 & \text{if tie-breaker predicts the price will increase} \\ 0 & \text{otherwise} \end{cases}$$

Fill in the below truth table for M.

P_3	P_2	P_1	P_0	M
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Question 1d. (15 pts)

Using a 4-to-1 multiplexer and multiple logic gates, design a circuit that implements M as shown in your truth table above. Simplify the inputs to the multiplexer as much as possible. You can directly use B as an input to any device. Explain your design.

Hint: Use P_3 and P_2 as selection bits.

Problem 2: Comparing robot distances (30pts)

Consider an autonomous delivery vehicle that receives a two-bit delivery address $A = (A_1A_0)_2$. Suppose the vehicle has *memory* so that it stores its most recent delivery location as a 2-bit binary number $L = (L_1L_0)_2$. The goal of this problem is to upgrade the delivery vehicle to be able to *compare the address* of a new order A with its most recent location L.

Question 2a. (5 pts)

Define the following logic signals:

$$F = \begin{cases} 1 & \text{if } (L)_{10} < (A)_{10}, \\ 0 & \text{otherwise,} \end{cases} \qquad G = \begin{cases} 1 & \text{if } (L)_{10} > (A)_{10} \\ 0 & \text{otherwise,} \end{cases} \qquad E = \begin{cases} 1 & \text{if } (L)_{10} = (A)_{10} \\ 0 & \text{otherwise.} \end{cases}$$

Fill in the following truth table for F, G, E.

A_1	A_0	L_1	L_0	F	G	E
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Question 2b. (5 pts)

Derive the simplest possible Boolean expressions for F and G using Karnaugh maps.

L_1L_0 \ A_1A_0	00	01	11	10
00				
01				
11				
10				

L_1L_0 \ A_1A_0	00	01	11	10
00				
01				
11				
10				

Question 2c. (10 pts)

Suppose that you restrict the location of the vehicle so that $L < 2$ in base-10, that is, L can only takes values $(00)_2$ or $(01)_2$.

1. Write the simplest possible Boolean expressions for F, G, and E.
2. Design a circuit using any devices of your choice that outputs F, G, and E; provide an explanation for your design.

Question 2d. (10 pts)

Suppose that data for new delivery addresses A are made available to the vehicle over time, shown bit-wise in Figure 1. *Assuming that the vehicle is parked at* $L = (01)_2$ *the entire time,* sketch the outputs for F and G as a function of time.

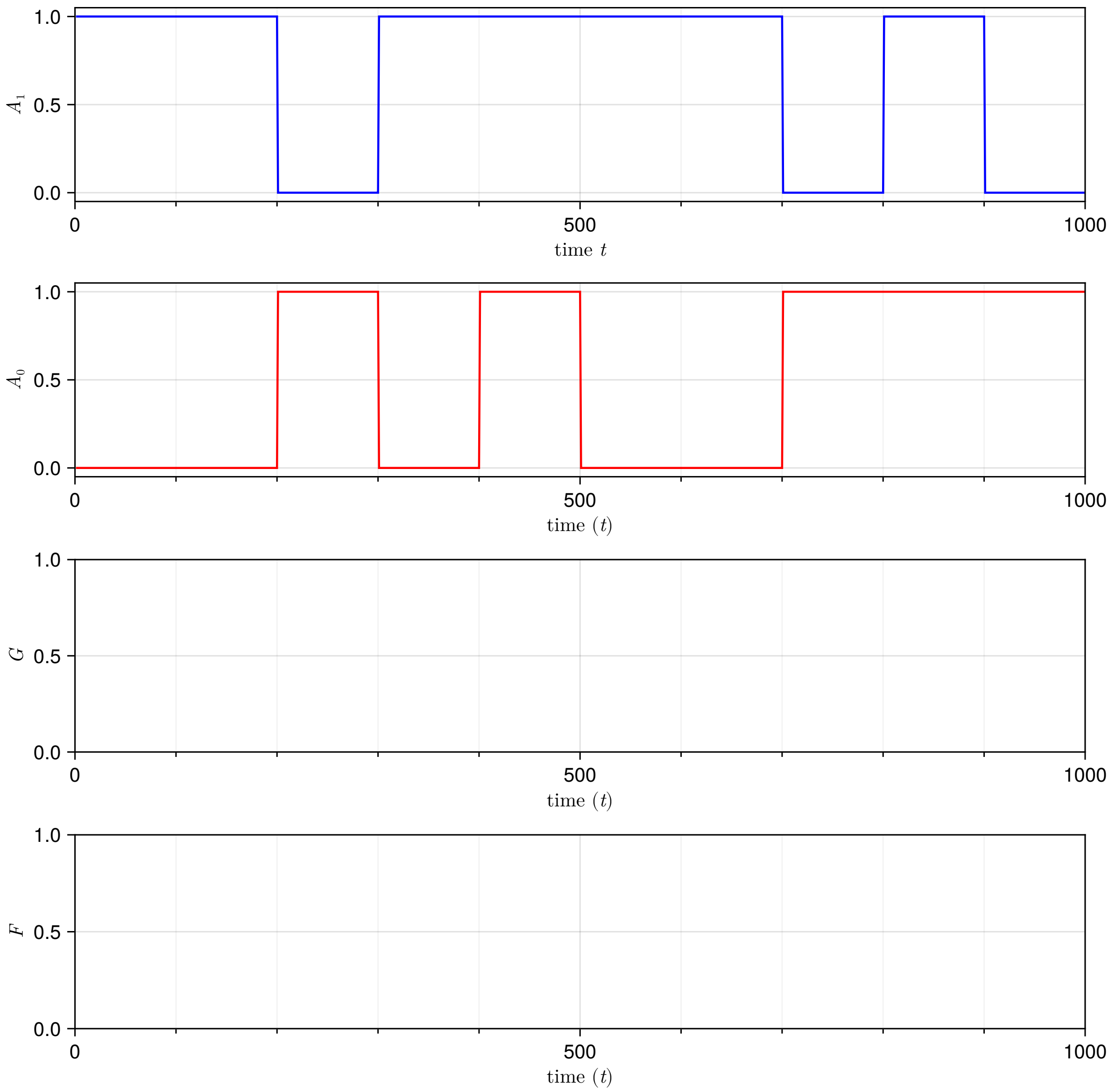

Figure 1: Sketch the outputs for F and G as a function of time

Problem 3: Number Systems (20pts)

Question 3a. (5 pts)

Perform the following calculation in 2's complement binary arithmetic and verify that your final result, converted to base-10, matches the expected value. *Show all working steps.*

$$(71 - 36)_{10}. \quad (3)$$

Question 3b. (5 pts)

Consider the following matrix with base-b entries:

$$\boldsymbol{A} = \begin{bmatrix} (121)_b & 0 \\ (4)_b & (11)_b \end{bmatrix}.$$

Suppose that $\boldsymbol{A}$ has *base-10* eigenvalues

$$\lambda_1 = (64)_{10} \quad \text{and} \quad \lambda_2 = (8)_{10}.$$

What is the value of b?

Hint: The eigenvalues of a triangular matrix are the entries on its diagonal.

Question 3c. (5 pts)

How many bits are required to fully represent the result of these summations in 2's complement?

1. $(10100111)_2 + (11100100)_2$
2. $(10010110)_2 + (10110011)_2$
3. $(01011100)_2 + (10110101)_2$

Question 3d. (5 pts)

Recall the full binary adder from class, which takes as inputs:

1. Binary logic signals X, Y,
2. Binary carry-in signal C_{in}

and returns the sum S and carry out C_{out}. Using no additional gates, explain how we can implement the function

$$Z(X,Y) = X \cdot Y$$

using only the inputs X, Y and the full adder circuit.

Problem 4: Concepts (10pts)

Question 4a. (2 pts)

Suppose that you want to implement a 16-to-1 multiplexer using 4-to-1 multiplexers. How many multiplexers would be required to do this? Answer: _______

Question 4b. (3 pts)

Name the building block devices that have these characteristics:

1. n input lines, 2^n output lines: _______
2. 1 input line, n selection lines, and 2^n output lines: _______
3. 2^n input lines, n selection lines, and 1 output line: _______

Question 4c. (5 pts)

Let X and Y be two base-10 numbers. Assume that you know the prices will satisfy

$$0 \leq X \leq 7$$
$$0 \leq Y \leq 7.$$

What is the minimum number of bits we need to represent any possible value of

$$F = X - Y$$

Scratch paper; if used, please clearly indicate which question you are working on