Digital System Design, Final Exam

ECE 2020-IE
12/05/2024-12/07/2024

Name: _____

I, _____, commit to uphold the ideals of honor and integrity by refusing to betray the trust bestowed upon me as a member of the Georgia Tech Community.

Please read this information:

- **This is a 48-hour take home exam.**
- **You have until 6:00 pm ET, Saturday, December 7th to submit this exam.**
- Do not collaborate or communicate with any other individuals during this exam. Do your own work. You are on your honor.
- Any instances of suspected collaboration will be reported to the Office of Student Integrity.
- You are responsible for the content of all your answers.
- Please show all your work.
- Please box or circle your final answers.
- This test has 5 problems that total up to 100 points.
- This test has 2 bonus questions that total up to 10 bonus points.

Boolean Identities

- Identity:
  - $A + 0 = A$
  - $A \cdot 1 = A$
- Dominance:
  - $A + 1 = 1$
  - $A \cdot 0 = 0$
- Idempotence:
  - $A + A = A$
  - $A \cdot A = A$
- Inverse:
  - $A + \overline{A} = 1$
  - $A \cdot \overline{A} = 0$
- Commutative:
  - $A + B = B + A$
  - $A \cdot B = B \cdot A$
- Associative:
  - $A + (B + C) = (A + B) + C$
  - $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- Distributive:
  - $A \cdot (B + C) = A \cdot B + A \cdot C$
  - $A + B \cdot C = (A + B) \cdot (A + C)$
- Absorption:
  - $A \cdot (A + B) = A$
  - $A + A \cdot B = A$
- DeMorgan's:
  - $\overline{(A + B)} = \overline{A} \cdot \overline{B}$
  - $\overline{(A \cdot B)} = \overline{A} + \overline{B}$
- Double Complement:
  - $\overline{\overline{A}} = A$
- FOIL:
  - $(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$
- Disappearing Opposite:
  - $A + \overline{A} \cdot B = A + B$

Exam wrapper (3 bonus points)

Question I. (1 pts)

Reflect on your work in preparation for this course by answering the following questions:

1. Approximately how many hours did you spend studying for this exam? _____
2. Please indicate what percentage of your time was spent on the components of the course:
   (a) Prepared course notes: _____
   (b) Lecture slides and handwritten notes: _____
   (c) Solving and resolving homework: _____
   (d) Researching material on my own: _____

Question II. (1 pts)

Reflect on the topics you believed were your strengths and weaknesses going into this exam. You don't need to use every blank space.

1. Which topic(s) did you feel the most confident about?
   (a) _____
   (b) _____
   (c) _____
2. What topic(s) did you feel the least confident about?
   (a) _____
   (b) _____
   (c) _____

Question III. (1 pts)

In your opinion, what was the most interesting part of this class?

_____

Problem 1: In Search of Primes (30pts)

Consider the following 4-bit binary number:

$$X = (ABCD)_2. \tag{1}$$

The goal of this problem is to design a logic circuit that determines *when the 4-bit binary number X is a prime number.*[1] The inputs to the logic circuit are the 4 bits A, B, C and D. The output of the logic circuit, P, is defined as

$$P = \begin{cases} 1 & \text{if } X \text{ is prime,} \\ 0 & \text{if } X \text{ is not prime.} \end{cases}$$

Recall that a number X is prime if it is not divisible by any number except itself and 1.

Question 1a. (4 pts)

Suppose that X is an **unsigned** binary number. What is the minimum and maximum base-10 value of X?

1. **Minimum** base-10 value of X: _____
2. **Maximum** base-10 value of X: _____

Question 1b. (4 pts)

Using your result from Question 1a., write all of the prime numbers that X can represent in unsigned binary.

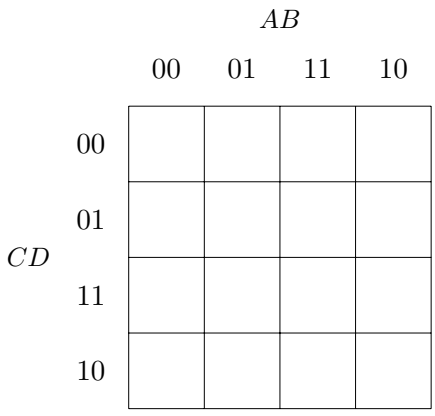
1. Base-10: _____, Binary (Unsigned): _____
2. Base-10: _____, Binary (Unsigned): _____
3. Base-10: _____, Binary (Unsigned): _____
4. Base-10: _____, Binary (Unsigned): _____
5. Base-10: _____, Binary (Unsigned): _____
6. Base-10: _____, Binary (Unsigned): _____

[1] **Fun fact to lighten the mood:** During *this semester*, on October 12, 2024, the largest known prime number was discovered: that number is $2^{136279841} - 1$, which broke a previous record from 2018. This gargantuan number was discovered by an ex-NVIDIA employee, who spent more than *$2 million USD of their personal funds* on compute—ironically, on an NVIDIA GPU—to achieve this feat. You can track the progress of this search here.

Question 1c. (7 pts)

Using your result from Question 1b., fill in the truth table below for the prime number detector, and derive the simplest possible expression for P using the 4×4 K-Map below.

A	B	C	D	P
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



Question 1d. (4 pts)

Now, suppose that X is a **2's complement** binary number. What is the minimum and maximum base-10 value of X?

1. **Minimum** base-10 value of X: _____
2. **Maximum** base-10 value of X: _____

Question 1e. (4 pts)

Using your result from Question 1d., write all of the prime numbers that X can represent in 2's complement binary. ***Note:*** *By definition, a negative number* ***cannot*** *be prime.*

1. Base-10: _____, Binary (2's comp.): _____
2. Base-10: _____, Binary (2's comp.): _____
3. Base-10: _____, Binary (2's comp.): _____
4. Base-10: _____, Binary (2's comp.): _____

Question 1f. (7 pts)

Using your result from Question 1e., derive the simplest possible Boolean expression for P using Boolean Algebra identities, assuming that X **is a 2's complement binary number**. Please show all of your work and box your final answer.

Problem 1 Bonus: Prime Detector Schematic (7 bonus pts)

Question 1g. (7 bonus pts)

Using your previous results from Problem 1, draw a circuit using a **4-to-16 Decoder** and logic gates, which has two outputs:

1. P_1: The value of P assuming X is an unsigned binary number.
2. P_2: The value of P assuming X is a 2's complement binary number.

Problem 2: Mystery Multiplexer (20pts)

Consider an unknown logic function $F(A, B, C, D)$ that is the output of a 4-to-1 multiplexer, where A and B are **the selector bits** of the multiplexer. Suppose that the truth table for F is given as in Table 1.

Table 1: Truth table for the unknown output F of a 4-to-1 multiplexer.

MUX input	A	B	C	D	F
I_0	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	1
	0	0	1	1	1
I_1	0	1	0	0	0
	0	1	0	1	0
	0	1	1	0	1
	0	1	1	1	1
I_2	1	0	0	0	1
	1	0	0	1	0
	1	0	1	0	1
	1	0	1	1	0
I_3	1	1	0	0	1
	1	1	0	1	1
	1	1	1	0	1
	1	1	1	1	1

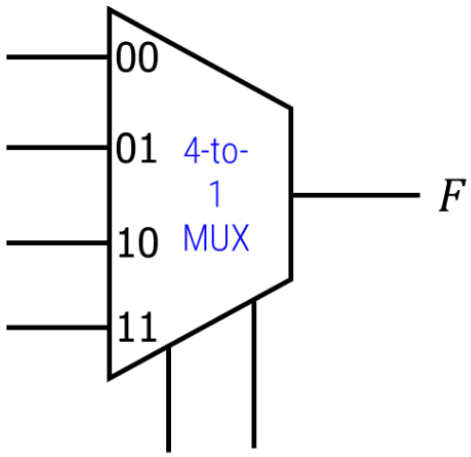
Question 2a. (8 pts)

Derive expressions for the multiplexer input signals I_0, I_1, I_2, and I_3.

1. $I_0 =$ _____
2. $I_1 =$ _____
3. $I_2 =$ _____
4. $I_3 =$ _____

Question 2b. (12 pts)

Using A and B as selector bits, draw a logic circuit that implements F using a 4-to-1 multiplexer and logic gates.



Problem 3: CMOS Circuit Design (20pts)

Consider a logic function F whose **complement** is given below in equation (2).

$$\overline{F} = \overline{A}B + C\left(A + \overline{D}\right). \tag{2}$$

Question 4a. (8 pts)

Derive Boolean expressions for the *pull-up* and *pull-down* network for F.
*Note: The **complement** of F is given in equation* (2).

1. Pull-up network: _____
2. Pull-down network: _____

Question 4b. (12 pts)

1. Draw a CMOS circuit that implements F. (8pts)
2. Label the pull-up and pull-down networks. (2pts)
3. Label the source, input, and output voltages using the symbols v_{dd}, v_{in}, and v_{out}, respectively. (2pts)

Problem 4: Number Systems (9pts)

Consider the following binary numbers:

1. 00100
2. 10011
3. 10100

Question 4a. (3 pts)

Assuming that the above binary numbers are **sign-magnitude** numbers, convert each of the numbers to base-10.

1. _____
2. _____
3. _____

Question 4b. (3 pts)

Assuming that the above binary numbers are **2's complement** numbers, convert each of the numbers to base-10.

1. _____
2. _____
3. _____

Question 4c. (3 pts)

Assume that the above binary numbers are now **unsigned fractional numbers**, where the fixed point is two places to the left. Specifically, the numbers now look like 001.00, 100.11, and 101.00, respectively. Convert each of the numbers to base-10.

1. _____
2. _____
3. _____

Problem 5: Sequential logic (21pts)

Question 5a. (3 pts)
What device corresponds to the timing diagram shown below in Fig. 1? (Circle one)

1. *D*-latch
2. Rising edge-triggered *D* flip-flop
3. Falling edge-triggered *D* flip-flop
4. None of the above

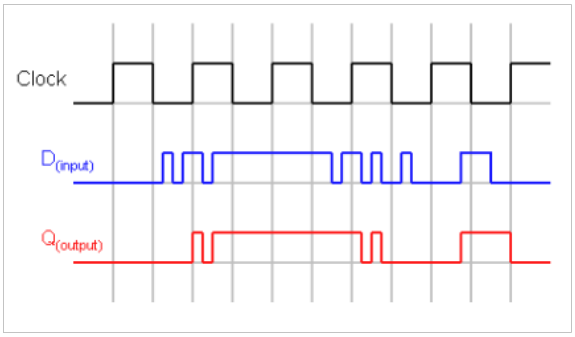


Figure 1: Timing diagram for Unknown Device 1

Question 5b. (3 pts)
What device corresponds to the timing diagram shown below in Fig. 2? (Circle one)

1. *D*-latch
2. Rising edge-triggered *D* flip-flop
3. Falling edge-triggered *D* flip-flop
4. None of the above

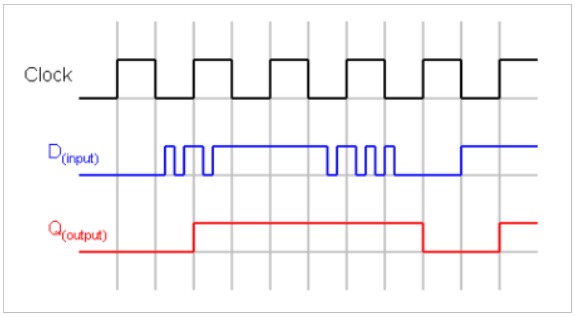


Figure 2: Timing diagram for Unknown Device 2

Question 5c. (3 pts)

Consider a finite state machine with one input: X, three state bits: Q_2, Q_1, Q_0, and a single output: Z. The expressions for the next state bits and the output Z are given as:

$$Q_0^+ = X$$
$$Q_1^+ = X + Q_2$$
$$Q_2^+ = XQ_1$$
$$Z = Q_2Q_0.$$

The finite state machine described above is (circle one):

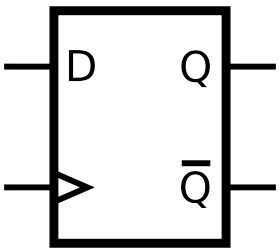
1. A Mealy Machine
2. A Moore Machine

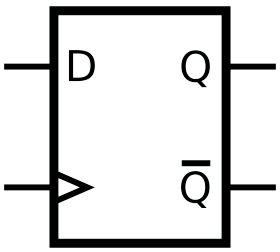
Question 5d. (2 pts)

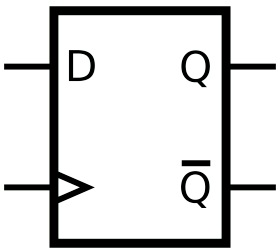
Suppose that the 3 state bits in Question 5c are in **compact encoding**. How many states are in the state machine? Answer: _____

Question 5e. (10 pts)

Draw a sequential logic circuit that implements the finite state machine described in Question 5c.







Scratch paper; if used, please clearly indicate which question you are working on