Problem Set #3

Autonomous last-mile delivery routing

Your startup is implementing an autonomous food delivery fleet at a large technical university campus. Since you have some knowledge of digital logic, you take the initiative to design a routing device that will be installed on each vehicle in the fleet. Each vehicle's routing device aims to determine whether a current order's delivery is possible, or whether the vehicle needs to be re-routed. This is done by selecting the correct path based on the binary address of the destination, using a multiplexer, a decoder, and basic binary number systems.

Inputs

In your prototype roll out, you select **4 drop-off locations** in your campus, each represented by a unique 2-bit binary address, which is represented as a binary address $A = (A_1 A_0)_2$. Your device receives the following information for each order:

- The drop-off location of the customer, represented by the two signals A_1, A_0.

- Path obstruction detection signals given by a radar sensor for each path R_3, R_2, R_1, R_0, which report the safety of the path to delivery at $(A_1 A_0)_{10}$:

$$R_i = \begin{cases} 1 & \text{path to location } i \text{ is not obstructed} \\ 0 & \text{otherwise.} \end{cases} \qquad i = (A_1 A_0)_{10}$$

Outputs

Your task is to design a routing device that outputs a *delivery-able* signal

$$D(A_1, A_0) = \begin{cases} 1 & \text{delivery to address } A_1 A_0 \text{ is possible} \\ 0 & \text{need re-routing} \end{cases}$$

Problem 1 (6 points)

Design a logic circuit using a 2-to-4 decoder, a 4-to-1 multiplexer, and 4 logic gates to return the routing feasibility signal D described above.

Multiplexers and Decoders: The Sequel

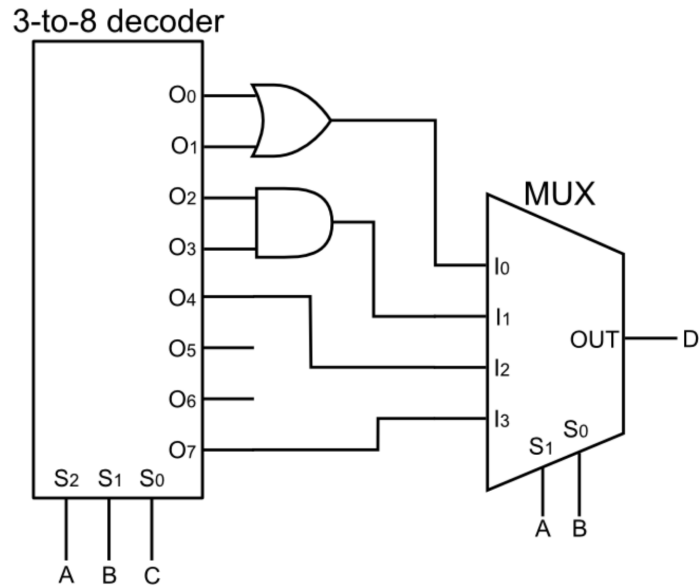Consider the following logic circuit using a 3-to-8 decoder and a 4-to-1 multiplexer.

Figure 1: A logic circuit that combines a decoder and multiplexer

The outputs of a 3-to-8 decoder $O_0, \ldots, O_7$ with selection control inputs S_2, S_1, S_0, have the form

$$O_i = \begin{cases} 1 & i = (S_2 S_1 S_0)_{10} \\ 0 & \text{otherwise.} \end{cases} \qquad i = 0, 1, \ldots, 7$$

The output signal D of the 4-to-1 multiplexer (MUX) with inputs I_0, I_1, I_2, I_3 and selection control inputs S_1, S_0 is given as

$$D = I_k \quad \text{where} \quad k = (S_1 S_0)_{10}.$$

Problem 2 (4 points)

Compute the simplest possible sum-of-products expression for the output

$$D = F(A, B, C)$$

shown in Fig. 1. Use a truth table and K-Map to verify your result.

Decoding the number system of an alien civilization

A few centuries in the future, you arise from cryogenic sleep orbiting in the Proxima Centauri system. You lead explorations to the Proxima Centauri b and Proxima Centauri d exoplanets, and shockingly, discover evidence of a previously existing multi-planetary civilization.

After decades of study, you amazingly find an artifact that indicates that the civilization knew how to solve quadratic equations. You are able to decode the following equation in an unknown base-b number system:

$$(5)_b x^2 - (50)_b x + (125)_b = 0 \implies x = (5)_b \text{ or } x = (8)_b$$

The value $x = (5)_b$ seems legitimate enough, but $x = (8)_b$ requires some further explanation, i.e., $b \neq 10$. You and your team reflect on the way that Earth's number system developed, and found evidence that the Proxima Centauri civilization had a similar history.

Problem 3 (4 points)

How many fingers did the extraterrestrials of the Proxima Centauri system most likely have? That is, what is the value of b?

Adder Chips in Real Life

Review the following data sheet for the 74HC283 adder chip:

Click for the data sheet for the 74HC283 adder chip

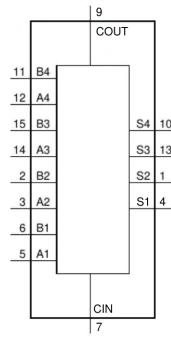The following functional diagram is a high-level depiction of this chip.

Figure 2: Functional diagram for the 74HC283 adder circuit

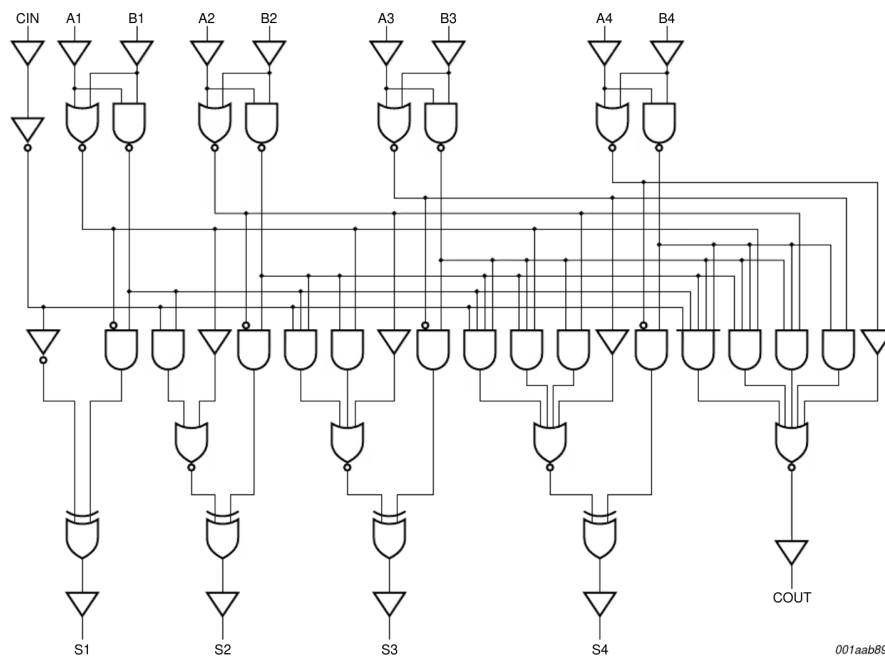Below, the entire logic circuit is depicted.

Figure 3: Full logic circuit for the 74HC283 adder circuit

Problem 4 (6 points)

Suppose you implement your 74HC283 chip in a project where the chip takes two 4-bit inputs $A := A_3 A_2 A_1 A_0$ and $B := B_3 B_2 B_1 B_0$, a single 1-bit *"carry-in"* input C_{in}. The circuit puts a 4-bit output *sum* $S := S_3 S_2 S_1 S_0$ and a 1-bit *"carry-out"* output C_{out}. Perform the following analyses of the adder chip.

1. Let the inputs be $A = 0101$, $B = 0111$, and $C_{in} = 0$. Compute the outputs S and C_{out} using binary arithmetic.

2. Suppose A and B are 4-bit unsigned integers. What is the range of possible base-10 integers that can be obtained by S, without consider C_{out}?

3. What is the range of possible base-10 integers that can be obtained by S, considering C_{out}?

Discovering properties of complement systems

Problem 5 (4 points)

Suppose that a $4n$-bit number B is represented by an n-digit hexadecimal number H.

1. Prove that the two's complement of B is represented by the 16s' complement of H.

2. Prove that the one's complement of B is represented by the 15s' complement of H

Hint: in a base b number system, the complement of any n-digit number $X = (D_{n-1}D_{n-2} \ldots D_1 D_0)_b$ can be obtained by subtracting it from b^n as

$$-X = b^n - \sum_{i=0}^{n-1} D_i \times b^i.$$

Cubes and Codes

Let $\mathcal{B}_n$ denote the n-dimensional *binary hypercube*[1]: $\mathcal{B}_n = \{\mathbf{u} : \mathbf{u} \in \{0,1\}^n\}$, which is the set of all n-dimensional binary vectors $\mathbf{u} \in \{0,1\}^n$.

Problem 6 (4 points, 1 bonus point possible)

Explore the following properties of hypercubes:

1. How many vertices, or unique vectors, are contained in $\mathcal{B}_n$? What do these represent? Explain in words. Then, write a formula that gives the number of m-dimensional sub-cubes of $\mathcal{B}_n$ for any values of m, n.

2. Consider the cases where $n = 3$ and $n = 4$. Draw the 3-dimensional and 4-dimensional hypercubes $\mathcal{B}_3$ and $\mathcal{B}_4$. For at least the $n = 3$ case, label the vertices, which represent all the natural numbers $\{0, 1, 2, \ldots, 7\}$ in binary.

3. **[BONUS] (1pt)** Use your drawing of $\mathcal{B}_4$ to draw a path along the edges that visits each vertex exactly once. Argue that this path orders the natural numbers $\{0, 1, 2, \ldots, 15\}$ represented by 4 bits while ensuring that only one bit changes at each step. What does this remind you of?

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[1]Hypercube

Working with number systems

Problem 7 (6 points)

Perform the following number system conversions.

1. Unsigned:

$$(1101)_2 = (?)_{10} \tag{1a}$$
$$(100111)_2 = (?)_{10} \tag{1b}$$
$$(10101.1001)_2 = (?)_{10} \tag{1c}$$
$$(36)_{10} = (?)_2 \tag{1d}$$
$$(132)_{10} = (?)_2 \tag{1e}$$
$$(11.75)_{10} = (?)_2 \tag{1f}$$
$$(ADC)_{16} = (?)_2 \tag{1g}$$
$$(CA)_{16} = (?)_8 \tag{1h}$$
$$(1010)_2 = (?)_8 \tag{1i}$$

2. Signed magnitude:

$$(100111)_2 = (?)_{10} \tag{2a}$$
$$(-86)_{10} = (?)_2 \tag{2b}$$

3. Two's complement:

$$(11101011)_2 = (?)_{10} \tag{3a}$$
$$(-77)_{10} = (?)_2 \tag{3b}$$

Binary arithmetic round 2

Problem 8 (6 points)

Perform signed two's complements binary arithmetic operations. Indicate whether overflow occured.

$$(0010010)_2 + (1001111)_2 = (?)_2 \tag{4a}$$
$$(0010010)_2 - (1001111)_2 = (?)_2 \tag{4b}$$
$$(0010010)_2 - (0110001)_2 = (?)_2 \tag{4c}$$