ECE 2020 IE3, Fall 2024

Problem Set #2

Due: September 17 (+2 bonus)
Hard Deadline: September 19

5 problems, 22 points possible

High-Speed Stock Trading Chip

You decide to design an ultra-high-speed stock trading device that can be electronically connected to the stock exchange of your choice. The device uses digital logic to make intelligent buy, sell, or hold decisions for a single stock based on price and volume.

Inputs

For each stock, you have two logic signals:

1. **Price indicator** P, where $P = 1$ if the stock price is increasing, and $P = 0$ if it's decreasing.
2. **Volume indicator** V, where $V = 1$ if the stock's trading volume is high (many people are trading the stock), and $V = 0$ if it is low (not many people are trading the stock).

Outputs

You want to design a hardware digital logic circuit that generates the following output signals based on the available indicator signals:

1. **Buy signal:** B, where $B = 1$ when the stock price is rising with high volume.
2. **Sell signal:** S, where $S = 1$ when the stock price is falling with high volume, *OR* the stock price is rising with low volume.
3. **Hold signal:** H, where $H = 1$ if neither the buy *nor* sell conditions are met.

Problem 1 ($4 \times 2 = 8$ points possible)

In this problem, we will design a hardware implementation of our stock trading mechanism.

1. In terms of P and V, derive expressions for the buy, sell, and hold signals B, S and H, respectively. Sketch the high-level switching logic for each signal, and a gate-level schematic for your entire trading device, without simplifying anything.

2. Derive the simplest possible expression for the hold signal H *in terms of P and V* using Boolean Algebra theorems. How many, and which logic gate(s) do we need to represent H in terms of P and V? Justify your answer with words.

3. In terms of P and V, what logic gate does the sell signal S represent? Justify your answer with a truth table.

4. Design a transistor-level CMOS circuit for your entire trading device that receives inputs of P and V and outputs B, S, and H. Indicate each of the pull-up and pull-down networks in the CMOS circuit.

   (Hint: Recall that CMOS logic uses a combination of PMOS and NMOS transistors to implement both the logic and its complement.)

5. **Bonus [2 points]:** How could you design an alert signal A, where $A = 1$ if buy and sell are not active at the same time? Give an electrical reason why this could be useful.

6. **Bonus [2 points]:** Suppose that you have no more than 4 stocks you are monitoring, and thus, you can represent everything in terms of 2 bit unsigned integers. Let H_1, H_2, H_3, H_4 be the hold signals from 4 copies of your trading device. Design a circuit that returns the sum of the hold signals. Explain your design.

Problem 1 Solution

P1.1

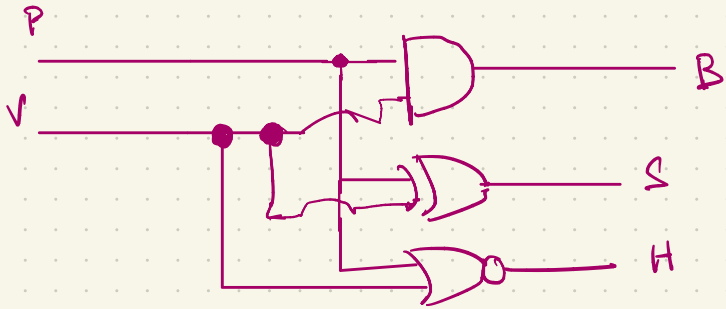
The buy and sell signals are simply $B = P \cdot V$ and $S = \overline{P} \cdot V + P \cdot \overline{V} = P \oplus V$, respectively.

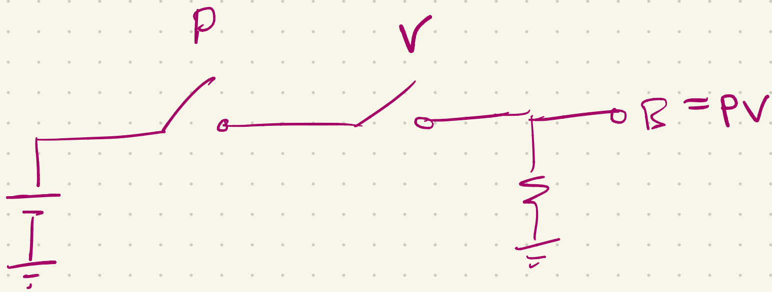
P1.2

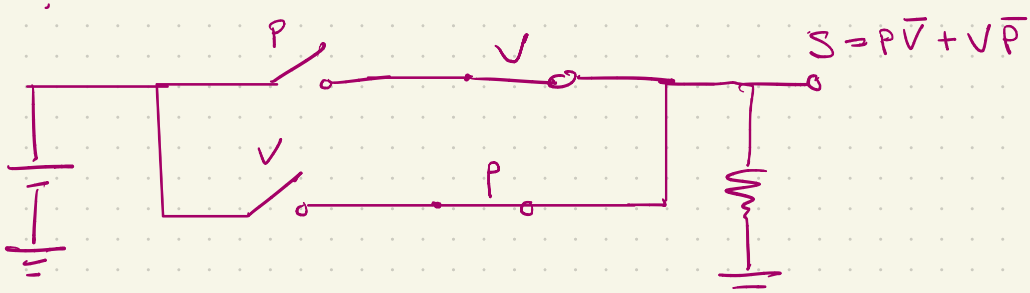
For the hold signal, we have that

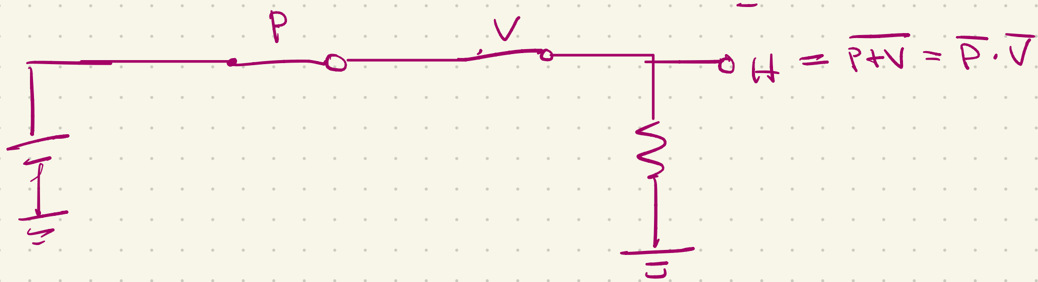
$$\begin{aligned} H &= \overline{B + S} \\ &= \overline{PV + \overline{P}V + \overline{V}P} \\ &= \overline{V(P + \overline{P}) + \overline{V}P} \\ &= \overline{V + \overline{V}P} \\ &\overset{(1)}{=} \overline{V + P}, \end{aligned}$$

where step (1) is by the Disappearing Opposite identity. Thus, we need a **single NOR gate** to represent the hold signal.


P
V
B
S
H


P
V
B = PV


P
V
V
P
S = PV̄ + VP̄


P
V
H = P̅+̅V̅ = P̄ · V̄

P1.3

As derived in part 1, $S = P \oplus V$, hence, the sell signal is an XOR gate.

P	V	S
0	0	0
0	1	1
1	0	1
1	1	0

P1.4

Buy signal:

1. Pull-up logic: $B(\overline{P}, \overline{V}) = \overline{P} \cdot \overline{V}$
2. Pull-down logic: $\overline{B(P, V)} = \overline{P} + \overline{V}$

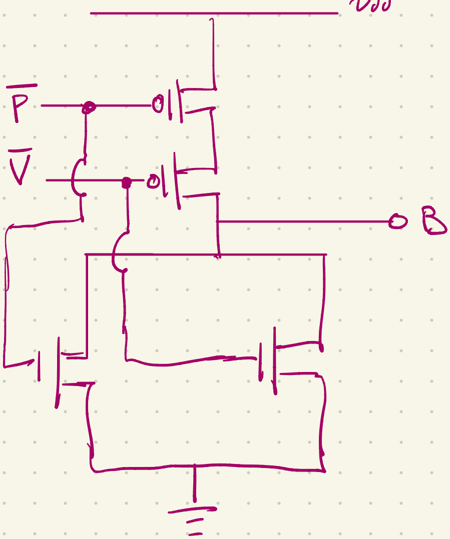
Sell signal:

1. Pull-up logic: $S(\overline{P}, \overline{V}) = \overline{P} \cdot V + P \cdot \overline{V}$
2. Pull-down logic: $\overline{S(P, V)} = \overline{\overline{P} \cdot V + P \cdot \overline{V}} = \overline{P} \cdot \overline{V} + V \cdot \overline{P}$ $= \underbrace{(\overline{P} + V) \cdot (\overline{V} + P)}_{\text{Also ok:}}$

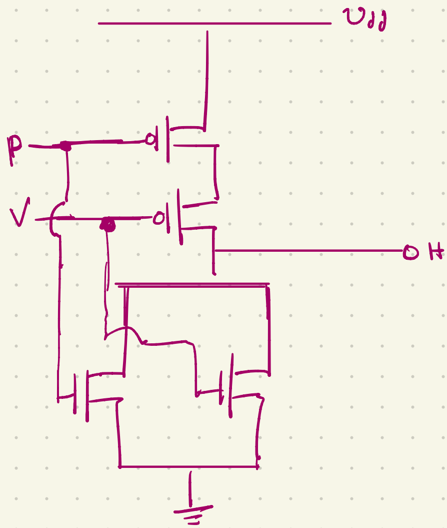
Hold signal:

1. Pull-up logic: $H(\overline{P}, \overline{V}) = P \cdot V$
2. Pull-down logic: $\overline{H(P, V)} = P + V$

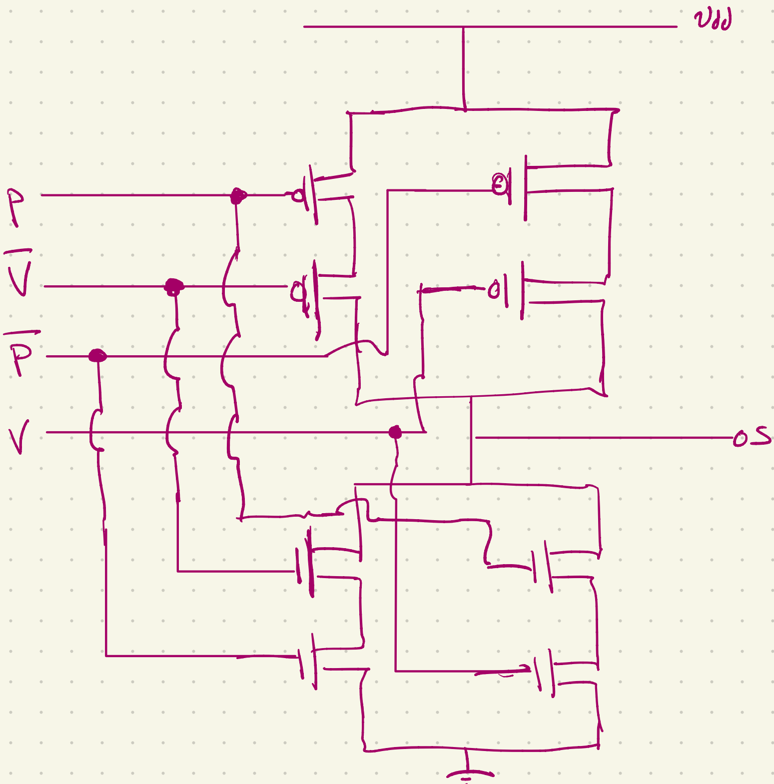
Buy:



Hold



Sell:



P1.5

One approach is to consider $A = \overline{BS}$. By monitoring how this signal evolves over time, we can detect timing hazards in the buy and sell signals.

P1.6

Let $\Sigma = H_1 + H_2 + H_3 + H_4$. Note that $0 \leq \Sigma \leq 4$. We can represent Σ as a two bit unsigned integer $\Sigma := \sigma_1\sigma_0$, where σ_1, σ_0 are binaries.

Let's first consider the sum $H_1 + H_2$. Note that

$$H_1 + H_2 = \begin{cases} 1 & H_1 = 1 \text{ and } H_2 = 1 \\ 1 & H_1 = 0 \text{ and } H_2 = 0 \\ 0 & H_1 \cdot H_2 = 0 \\ 0 & H_1 \cdot H_2 = 1 \quad \leftarrow \text{(carry out!)} \end{cases}$$

We need to *carry out* the sum to the next binary digit place if $H_1 \cdot H_2 = 1$. Thus, let $C_{\text{out},12} = H_1 \cdot H_2$, and $\Sigma_{12} := H_1 \oplus H_2$. Repeating this logic for the next two pairs of hold signals, it follows that Σ can be represented as $\Sigma := \Sigma_{12} + \Sigma_{34}$.

A useful mnemonic

We say that a logic function F is in *sum-of-products* (SOP) form when it is the logical sum of logical product terms. For example, the following logic function is in SOP form:

$$F_{\mathsf{SOP}} = X \cdot Y + \overline{Y} \cdot Z + \overline{Z} \cdot \overline{X}.$$

In contrast, this function is *not* in SOP form and needs to be simplified:

$$F_{\overline{\mathsf{SOP}}} = \overline{(Z \cdot (Y + \overline{Y} \cdot X))} + X \cdot Y \cdot Z$$

Problem 2 ($2 \times 2 = 4$ points possible)
In this problem, we will practice more with SOP forms.

1. Derive the simplest SOP forms of the following logic functions.
2. Build a truth table to show all possible combinations of input-output conditions. Indicate the SOP terms and sketch a logic gate-level schematic for the SOP expression (if there is more than one input for your simplified expression).

$$F_1 = \overline{X} \cdot (\overline{Y} \cdot Z + Y \cdot Z + Y \cdot \overline{Z}) + X \cdot Y \cdot Z \tag{1a}$$
$$F_2 = Y \cdot Z + \overline{Z} \cdot Y + X \cdot Y \tag{1b}$$
$$F_3 = \overline{X \cdot (\overline{Y} \cdot \overline{Z} + Y \cdot Z)} \tag{1c}$$

Problem 2 Solution

P2.A

We have

$$\begin{aligned}
F_1 &= \overline{X} \cdot \left(\overline{Y} \cdot Z + Y\left(Z + \overline{Z}\right)\right) + X \cdot Y \cdot Z \\
&= \overline{X} \cdot \left(\overline{Y} \cdot Z + Y\right) + X \cdot Y \cdot Z \\
&= \overline{X} \cdot (Y + Z) + X \cdot Y \cdot Z \\
&= \overline{X} \cdot Y + \overline{X} \cdot Z + X \cdot Y \cdot Z \\
&= \overline{X} \cdot Y + \left(\overline{X} + X \cdot Y\right) \cdot Z \\
&= \overline{X} \cdot Y + \overline{X} \cdot Z + Y \cdot Z,
\end{aligned}$$

where the third equality and the final equality are by the Disappearing Opposite identity.

P2.B

This problem is not graded, I made a typo that persisted in original version until too close to the deadline. You are encouraged to verify:

$$\begin{aligned} F_2 &= Y(Z+\overline{Z}) + XY \\ &= Y + XY \\ &= Y(1+X) \\ &= Y \end{aligned}$$

P2.C

We have

$$F_3 = \overline{X \cdot (\overline{Y} \cdot \overline{Z} + Y \cdot Z)} \tag{2}$$
$$\stackrel{(1)}{=} \overline{X} + \overline{(\overline{Y} \cdot \overline{Z} + Y \cdot Z)} \tag{3}$$
$$\stackrel{(2)}{=} \overline{X} + \overline{(\overline{Y} \cdot \overline{Z})} \cdot \overline{(Y \cdot Z)} \tag{4}$$
$$\stackrel{(3)}{=} \overline{X} + (Y+Z) \cdot (\overline{Y} + \overline{Z}) \tag{5}$$
$$= \overline{X} + Y\overline{Y} + Y\overline{Z} + Z\overline{Y} + Z\overline{Z} \tag{6}$$
$$= \overline{X} + Y\overline{Z} + Z\overline{Y}, \tag{7}$$

where steps (1), (2), and (3) are all by DeMorgan's theorem, and the subsequent steps are by FOIL and the fact that $A\overline{A} = 0$.

CMOS Circuit Design

Problem 3 ($2 \times 2 = 4$ points possible)
Consider the following logic function:

$$F(X, Y, Z) = \overline{(X \cdot \overline{\overline{Y} \cdot Z})}. \tag{8}$$

In this problem we will use NMOS and PMOS transistors to take this logic function to the real world in the form of a CMOS circuit.

1. Derive expressions for pull-up (PMOS)/pull-down (NMOS) switching networks.
2. Draw a schematic for the CMOS implementation of the logic function F. Indicate where the pull-up and pull-down networks are located in your schematic.

Assume that both the inputs and their complements are available (i.e., you can use inputs like $\overline{Z}$ directly without using an inverter).

Problem 3 Solution

P3A

The pull-up network logic is given as

$$F(\overline{X}, \overline{Y}, \overline{Z}) = \overline{(\overline{X} \cdot \overline{Y \cdot \overline{Z}})} \overset{(1)}{=} \overline{\overline{X}} + \overline{\overline{(Y \cdot \overline{Z})}} = X + Y \cdot \overline{Z},$$

where step (1) is by DeMorgan's Theorem. The pull-down network logic is given as

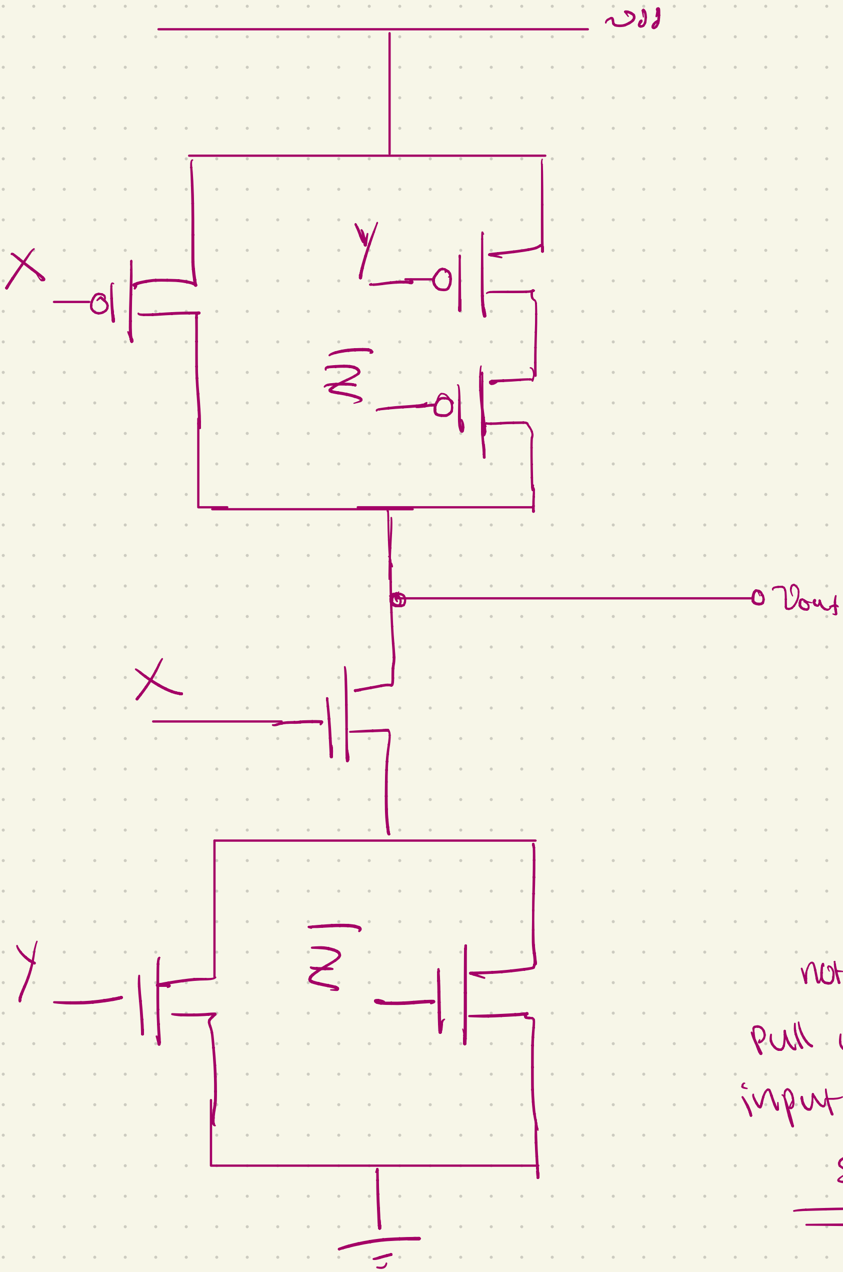
$$\overline{F(X, Y, Z)} = X \cdot \overline{\overline{Y} \cdot Z} = X \cdot (Y + \overline{Z}),$$

where final equality is also by DeMorgan's Theorem.

Because I gave everyone a few more days to correct your homework, you missed 0.5/2 points if you forgot to complement the inputs on the pull-up network.

P3B

3b.



note that
pull up & pull down
inputs are the
same

Karnaugh Maps (K-Maps)

Problem 4 ($2 \times 2 = 4$ points possible)

Consider a logic function F with four binary inputs A, B, C, D. Suppose that we define F in words as

$$F = \begin{cases} 1 & \text{at least two inputs are true} \\ 0 & \text{otherwise.} \end{cases}$$

1. Complete the truth table for F.

2. Using your completed truth table, construct a Karnaugh map using the 16-cell table labeled with gray codes below. Then, derive the most simplified SOP expression for F and draw a logic gate-level schematic.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	1	1	1	1
10	0	1	1	1

$$F = AB + CD + BD + BC + AD + AC.$$

Circuit identification practice

Problem 5 (2 points possible)
Identify the equivalent Boolean Algebra expression for the output voltage of the following CMOS circuit. *Hint: does the pull-up or pull-down network control the un-complemented output?*

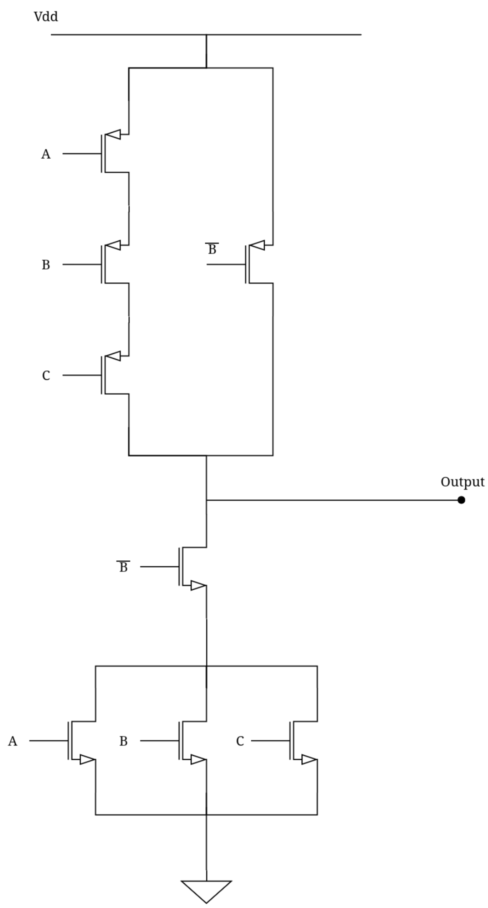


Figure 1: The CMOS circuit in question. Note that we only have PMOS on the pull-up network and NMOS on the pull-down network.

The logic for the output function is the same as the logic for the pull-up network with the shown inputs **complemented.** That is,

$$F = \overline{A} \cdot \overline{B} \cdot \overline{C} + B.$$

Because there was additional time to submit the homework, you missed 1/2 points if you did not un-complement the inputs.

Problem 6 (**BONUS**: 2 bonus points possible)
Let $X, Y \in \{0, 1\}$ be two logic signals. Prove DeMorgan's Theorems:

$$\overline{X+Y} = \overline{X} \cdot \overline{Y} \tag{9a}$$
$$\overline{X \cdot Y} = \overline{X} + \overline{Y} \tag{9b}$$

using Boolean Algebra identities (not using truth tables as we did in class). Justify every step and use text to explain.

Bonus Problem

For equation (9a), we want to show that $\overline{X+Y} = \overline{X} \cdot \overline{Y}$. We will do this via the inverse axiom (you can use the complementarity axiom as well) i.e., for any logic signal $X \in \{0, 1\}$ we have

$$X \cdot \overline{X} = 0;$$

thus, if our desired equality is true, it is necessary that the following equation is true:

$$(\overline{X} \cdot \overline{Y}) \cdot \overline{\overline{(X+Y)}} = (\overline{X} \cdot \overline{Y}) \cdot (X+Y) = 0.$$

Distributing, we claim that

$$\underbrace{\overline{X} \cdot \overline{Y} \cdot X}_{=0 \cdot \overline{Y}} + \underbrace{\overline{X} \cdot \overline{Y} \cdot Y}_{=\overline{X} \cdot 0} = 0,$$

which is clearly a true statement.

Note this is only a *necessary* condition. To prove a *necessary and sufficient* condition, we need to show that the statements of DeMorgan's Theorems implies that *all* of the **axioms** of Boolean algebra (things that are taken without proof), are satisfied.

These axioms are given as follows:

1. $X = 0 \implies X \neq 1, \qquad X = 1 \implies X \neq 0$
2. $X = 0 \implies \overline{X} = 1, \qquad X = 1 \implies \overline{X} = 0$
3. $0 \cdot 0 = 0, \qquad 1 + 1 = 1$
4. $1 \ldots 1 = 1, \qquad 0 + 0 = 0$
5. $0 \cdot 1 = 1 \cdot 0 = 0, \qquad 1 + 0 = 0 + 1 = 1$

Duality principle: By the above axioms, any identity in switching algebra remains true if 0 and 1 are swapped and $\cdot$ and $+$ are swapped throughout, therefore DeMorgan's Theorem is true.