High-Speed Stock Trading Chip

You decide to design an ultra-high-speed stock trading device that can be electronically connected to the stock exchange of your choice. The device uses digital logic to make intelligent buy, sell, or hold decisions for a single stock based on price and volume.

Inputs

For each stock, you have two logic signals:

1. **Price indicator** P, where $P = 1$ if the stock price is increasing, and $P = 0$ if it's decreasing.
2. **Volume indicator** V, where $V = 1$ if the stock's trading volume is high (many people are trading the stock), and $V = 0$ if it is low (not many people are trading the stock).

Outputs

You want to design a hardware digital logic circuit that generates the following output signals based on the available indicator signals:

1. **Buy signal:** B, where $B = 1$ when the stock price is rising with high volume.
2. **Sell signal:** S, where $S = 1$ when the stock price is falling with high volume, *OR* the stock price is rising with low volume.
3. **Hold signal:** H, where $H = 1$ if neither the buy *nor* sell conditions are met.

Problem 1 ($4 \times 2 = 8$ points possible)

In this problem, we will design a hardware implementation of our stock trading mechanism.

1. In terms of P and V, derive expressions for the buy, sell, and hold signals B, S and H, respectively. Sketch the high-level switching logic for each signal, and a gate-level schematic for your entire trading device, without simplifying anything.

2. Derive the simplest possible expression for the hold signal H *in terms of* P *and* V using Boolean Algebra theorems. How many, and which logic gate(s) do we need to represent H in terms of P and V? Justify your answer with words.

3. In terms of P and V, what logic gate does the sell signal S represent? Justify your answer with a truth table.

4. Design a transistor-level CMOS circuit for your entire trading device that receives inputs of P and V and outputs B, S, and H. Indicate each of the pull-up and pull-down networks in the CMOS circuit.

   (Hint: Recall that CMOS logic uses a combination of PMOS and NMOS transistors to implement both the logic and its complement.)

5. **Bonus [2 points]:** How could you design an alert signal A, where $A = 1$ if buy and sell are not active at the same time? Give an electrical reason why this could be useful.

6. **Bonus [2 points]:** Suppose that you have no more than 4 stocks you are monitoring, and thus, you can represent everything in terms of 2 bit unsigned integers. Let H_1, H_2, H_3, H_4 be the hold signals from 4 copies of your trading device. Design a circuit that returns the sum of the hold signals. Explain your design.

A useful mnemonic

We say that a logic function F is in *sum-of-products* (SOP) form when it is the logical sum of logical product terms. For example, the following logic function is in SOP form:

$$F_{\mathsf{SOP}} = X \cdot Y + \overline{Y} \cdot Z + \overline{Z} \cdot \overline{X}.$$

In contrast, this function is *not* in SOP form and needs to be simplified:

$$F_{\overline{\mathsf{SOP}}} = \overline{(Z \cdot (Y + \overline{Y} \cdot X))} + X \cdot Y \cdot Z$$

Problem 2 ($2 \times 2 = 4$ points possible)
In this problem, we will practice more with SOP forms.

1. Derive the simplest SOP forms of the following logic functions.
2. Build a truth table to show all possible combinations of input-output conditions. Indicate the SOP terms and sketch a logic gate-level schematic for the SOP expression (if there is more than one input for your simplified expression).

$$F_1 = \overline{X} \cdot (\overline{Y} \cdot Z + Y \cdot Z + Y \cdot \overline{Z}) + X \cdot Y \cdot Z \tag{1a}$$

$$F_2 = Y \cdot Z + \overline{Z} \cdot Y + X \cdot Y \tag{1b}$$

$$F_3 = \overline{X \cdot (\overline{Y} \cdot \overline{Z} + Y \cdot Z)} \tag{1c}$$

CMOS Circuit Design

Problem 3 ($2 \times 2 = 4$ points possible)
Consider the following logic function:

$$F(X, Y, Z) = \overline{(X \cdot \overline{\overline{Y} \cdot Z})}. \tag{2}$$

In this problem we will use NMOS and PMOS transistors to take this logic function to the real world in the form of a CMOS circuit.

1. Derive expressions for pull-up (PMOS)/pull-down (NMOS) switching networks.
2. Draw a schematic for the CMOS implementation of the logic function F. Indicate where the pull-up and pull-down networks are located in your schematic.

Assume that both the inputs and their complements are available (i.e., you can use inputs like $\overline{Z}$ directly without using an inverter).

Karnaugh Maps (K-Maps)

Problem 4 ($2 \times 2 = 4$ points possible)

Consider a logic function F with four binary inputs A, B, C, D. Suppose that we define F in words as

$$F = \begin{cases} 1 & \text{at least two inputs are true} \\ 0 & \text{otherwise.} \end{cases}$$

1. Complete the truth table for F.
2. Using your completed truth table, construct a Karnaugh map using the 16-cell table labeled with gray codes below. Then, derive the most simplified SOP expression for F and draw a logic gate-level schematic.

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

AB \ CD	00	01	11	10
00				
01				
11				
10				

Here is a good resource on Karnaugh Maps, we'll talk more about these the week of 09/08.

Circuit identification practice

Problem 5 (2 points possible)

Identify the equivalent Boolean Algebra expression for the output voltage of the following CMOS circuit. *Hint: does the pull-up or pull-down network control the un-complemented output?*

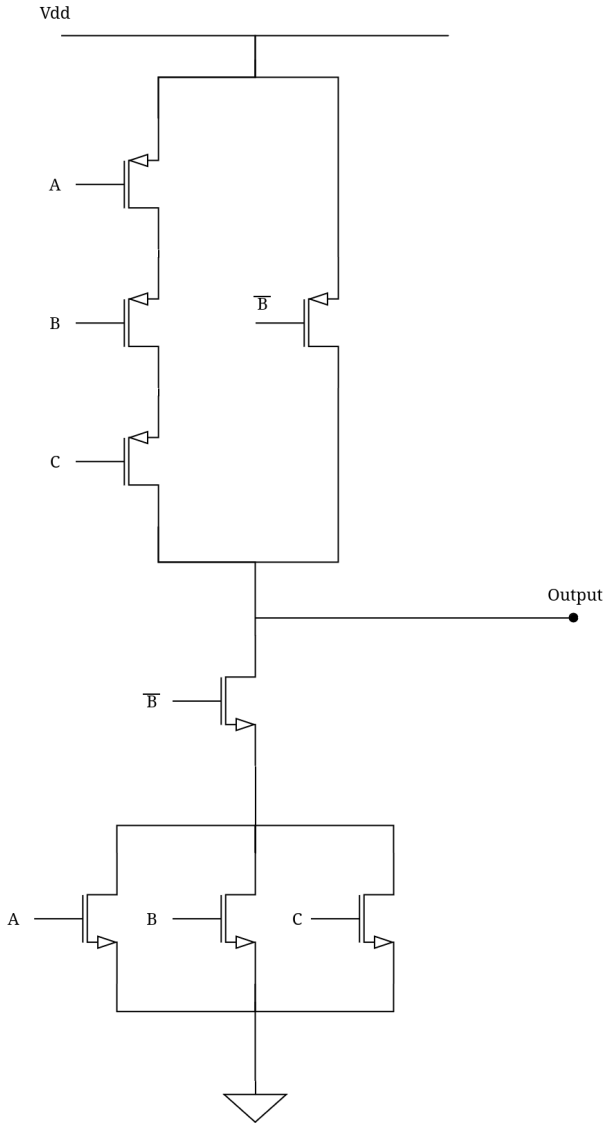

Figure 1: The CMOS circuit in question. Note that we only have PMOS on the pull-up network and NMOS on the pull-down network.

Problem 6 (**BONUS**: 2 bonus points possible)
Let $X, Y \in \{0, 1\}$ be two logic signals. Prove DeMorgan's Theorems:

$$\overline{X + Y} = \overline{X} \cdot \overline{Y} \tag{3a}$$

$$\overline{X \cdot Y} = \overline{X} + \overline{Y} \tag{3b}$$

using Boolean Algebra identities (not using truth tables as we did in class). Justify every step and use text to explain.