

Week of	Topics	Approximate textbook sections			
		Wakerly 4th	Wakerly 5th	Willis and Willis	Harris and Harris
18-Aug	Class logistics and introduction Boolean logic and expressions Switches and switch networks	1.2, 1.4 4.0-4.1 3.1	1.2, 1.4 3.0-3.1	BA SW	1.1-1.3, 2.1 2.2
25-Aug	Algebraic manipulation and simplification Transistors, logic levels, CMOS Gate-level design	4.1 3.3 1.3, 3.1, 4.2, 6.1.2, 6.1.7	1.9, 14.1-2 1.5, 3.2, 4.1.2	GD	2.3 1.6, 1.7 1.4, 2.4
1-Sep	(Monday holiday) Mixed-logic notation and manipulation Logic simplification with K-maps & SoP	4.3.2, 6.1.3-5 2.11, 4.1.6, 4.3.3-5	3.3.2, 4.1.3-6 2.11, 3.3.3	GD BA, SP	2.5 2.2.2, 2.7
8-Sep	Circuit timing Lab 1: Combinational circuits	3.6, 4.4, 6.2 1.6, 3.2, 3.4-5	3.4, 4.2, 14.4 1.7		2.9
15-Sep	Number systems (representations, bases, math) Test 1: Digital logic and implementation, 19-Sep	2.0-2.4	2.0-2.3	NS, AR	1.4, 5.3
22-Sep	Number systems (negatives, fractions) Building blocks; adders, subtractors Encoders, decoders, implementation and uses	2.5-2.7 6.1.1, 6.1.8, 6.10 6.4, 6.5	2.4-2.7 6.1, 4.1.1, 4.1.8-9, 8.1 6.3	NS BB	5.2
29-Sep	Muxes, demuxes, implementation and uses Latches & Flip-flops	3.7.1, 3.7.3, 6.7 7.0-7.2	6.4, 7.1 10.1-10.2	BB LR	1.7.7, 2.8.1-2 3.2
6-Oct	Finite state machines Test 2: Numbers; Building blocks, 10-Oct	7.3-4	9.1, 9.5		3.1, 3.4
13-Oct	(Monday/Tuesday holiday) Designing FSM behavior Physical FSM implementation	7.5 7.6-7.7	9.3		
20-Oct	Flip-flop and state machine timing FSM architectures Lab 2: Finite state machines	8.1.4	9.2, 13.1		3.5
27-Oct	Memory and data storage Memory block combination	6.6, 9.1	7.1, 15.1-3		2.6, 5.5
3-Nov	Test 3: Sequential logic, memory, processors 7-Nov Datapath elements				5.2.4, 5.5.5
10-Nov	Single-cycle datapath; Microcode Processor architecture				7.1-3
17-Nov	Low-level programming				6.*
24-Nov	Test 4: Optional redemption exam, 26-Nov (Wednesday-Friday holiday)				
1-Dec	Course review Final Exam: Cumulative, (Thurs. 5-Dec, 6:00 PM)				